2836  
PATENT

## UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Kemp

Attorney Docket No.: TRIPP013

Application No.: 09/738,267

Examiner: Nguyen, Danny

Filed: December 15, 2000

Group: 2836

Title: OVERVOLTAGE PROTECTION  
CIRCUIT

## CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail to: Commissioner for Patents, Washington, DC 20231 on March 27, 2003.

Signed: 

Mia Mitchell-Haynes

AMENDMENT TRANSMITTALCommissioner for Patents  
Washington, DC 20231

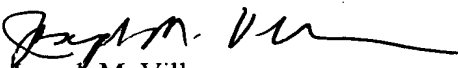
Sir:

Transmitted herewith is an Amendment in the above-identified application.

The fee has been calculated as shown below.

	Claims After Amendment		Highest Previously Paid For	Present Extra	Small Entity Rate Fee	Large Entity Rate Fee
Total Claims	10	MINUS	12	0	x 9 =	x 18 = 0
Independent Claims	4	MINUS	4	0	x 42 =	x 84 = 0
Multiple Dependent Claim Present and Fee Not Previously Paid					\$140.00	\$280.00
Total					\$	\$0

- ☐ Applicant(s) hereby petition for a \_\_\_\_\_ extension(s) of time to respond to the aforementioned Office Action.
- ☒ Applicant(s) believe that no (additional) Extension of Time is required; however, if it is determined that such an extension is required, Applicant(s) hereby petition that such an extension be granted and authorize the Commissioner to charge the required fees for an Extension of Time under 37 CFR 1.136 to Deposit Account No. 500388.
- ☐ Enclosed is our Check No. \_\_\_\_\_ in the amount of \$ \_\_\_\_\_ to cover the additional claim fee and/or extension of time fees.
- ☒ Please charge the required fees, or any additional fees required to facilitate filing the enclosed response, to Deposit Account No. 500388 (Order No. TRIPP013).

Respectfully submitted,  
BEYER WEAVER & THOMAS, LLP  
Joseph M. Villeneuve  
Reg. No. 37,460P.O. Box 778  
Berkeley, CA 94704-0778RECEIVED  
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#10/13  
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CERTIFICATE OF MAILING

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Signed: \_\_\_\_\_

Mia Mitchell-Haynes

RESPONSE

Commissioner for Patents  
Washington, D.C. 20231

Dear Sir:

This paper is filed in response to the Office Action dated February 18, 2003.

Reconsideration of the currently pending claims (reproduced in the attached appendix) is respectfully requested.

REMARKS

Claims 1-7 and 10-12 are currently pending in the application. Claims 1-7 and 10-12 were rejected. The Examiner rejected claims 1-7 and 10-12 under 35 U.S.C. 102(a) as being anticipated by U.S. Patent No. 5,929,615 (D'Angelo). The rejection is respectfully traversed.

Beginning at column 3, line 60, and referring to Fig. 2, D'Angelo describes a voltage regulator circuit 32 which performs both step-up and step-down regulation functions. A PMOS transistor 34 is connected between an input voltage terminal VIN (via inductor 36) and a regulated output voltage terminal VOUT. The operation of transistor 34 (as well as NMOS

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